Claims:

1(Previously amended). A stack having a stack depth configured in a nonvolatile memory to store parameter values, where each memory write invalidates previous data.

2(Original). The stack of claim 1 wherein the nonvolatile memory includes a pair of blocks that are erased independently.

3(Original). The stack of claim 2 wherein valid parameter values are stored in a first block of the pair of blocks and a second block is erased.

4(Original). The stack of claim 3 wherein valid parameter values are stored in the second block of the pair of blocks and the first block is erased.

5(Original). The stack of claim 1 further including a register to store an offset value used to generate an address for words in the nonvolatile memory.

6(Original). The stack of claim 1 further including a smart stack controller to dynamically determine a number of blocks used in the stack.

7(Original). The stack of claim 1 further including a smart stack controller to distribute write cycles across multiple blocks of the nonvolatile memory.

8-10(Canceled).

11(Previously amended). A nonvolatile stack to store parameter values in words of a nonvolatile memory where a write of the nonvolatile stack invalidates previous instructions or data stored in the nonvolatile stack.

12(Previously amended). The nonvolatile stack of claim 11, wherein a memory pool in at least first and second blocks of the nonvolatile memory are sized to balance cycling and data retention capabilities with a write specification.

13(Previously amended). The nonvolatile stack of claim 11, further including a stack controller to distribute write cycles across multiple blocks of the nonvolatile memory.

14(Previously amended). The nonvolatile stack of claim 11, wherein the nonvolatile memory maps a received address to determine memory blocks to be written.

15-31(Canceled).

32. The stack of claim 1 wherein the nonvolatile memory is a polymer memory that includes ferroelectric memory cells.